COURSE OUTLINE

(1) GENERAL

SCHOOL	ENGINEERING		
ACADEMIC UNIT	ELECTRICAL AND COMPUTER ENGINEERING DEPT.		
LEVEL OF STUDIES	Undergraduate		
COURSE CODE	**ECE_ELE830**	**SEMESTER**	**8**
COURSE TITLE	Hardware Description Languages (HDL)		

INDEPENDENT TEACHING ACTIVITIES *if credits are awarded for separate components of the course, e.g. lectures, laboratory exercises, etc. If the credits are awarded for the whole of the course, give the weekly teaching hours and the total credits*	**WEEKLY TEACHING HOURS**	**CREDITS**
Lectures	2	
Seminars / Practice exercises	1	
Laboratory	1	
Add rows if necessary. The organisation of teaching and the teaching methods used are described in detail at (4).	4	5

COURSE TYPE *general background, special background, specialised, general knowledge, skills development*	Specialised
PREREQUISITE COURSES:	No. Students are advised to have already attended the courses: • Digital Logic (ECE_K140) • Digital Circuit and Systems (ECE_K450)
LANGUAGE OF INSTRUCTION and EXAMINATIONS:	Greek
IS THE COURSE OFFERED TO ERASMUS STUDENTS	Yes.
COURSE WEBSITE (URL)	https://www.ece.uop.gr/

(2) LEARNING OUTCOMES

Learning outcomes

The course learning outcomes, specific knowledge, skills and competences of an appropriate level, which the students will acquire with the successful completion of the course are described.

Consult Appendix A

- *Description of the level of learning outcomes for each qualifications cycle, according to the Qualifications Framework of the European Higher Education Area*
- *Descriptors for Levels 6, 7 & 8 of the European Qualifications Framework for Lifelong Learning*

and Appendix B

- *Guidelines for writing Learning Outcomes*

In this course, the Hardware Description Language named VHDL is taught. Initially, the model levels of a digital circuit in VHDL and the basic blocks in VHDL such as Entity, Architecture, Process, Data Types, Operators, Packages and Libraries, Procedures and Functions, Properties are given in details. Then, the description for sequential, combinatorial circuits as well as the structural description type are given. Also, the workflow of implementation of digital circuit is given. In addition, the concepts about compilation, simulation and hierarchical design are described. The basics about parameterized VHDL code are given. Finally, some notes about code for logic synthesis, circuits for signal processing as well as mixed VHDL codes are given.

Learning outcomes

Upon successful completion of the course, students will be able to:

- Knows the parts of the VHDL code
- Uses VHDL building blocks
- Simulate circuits designed with VHDL
- Writes code for combinational circuits
- Writes code for sequential circuits
- Implements complex digital systems with VHDL
- Combines VHDL code types

General Competences

Taking into consideration the general competences that the degree-holder must acquire (as these appear in the Diploma Supplement and appear below), at which of the following does the course aim?

Search for, analysis and synthesis of data and information, with the use of the necessary technology	*Project planning and management*
Adapting to new situations	*Respect for difference and multiculturalism*
Decision-making	*Respect for the natural environment*
Working independently	*Showing social, professional and ethical responsibility and sensitivity to gender issues*
Team work	*Criticism and self-criticism*
Working in an international environment	*Production of free, creative and inductive thinking*
Working in an interdisciplinary environment	*……*
Production of new research ideas	*Others…*
	…….

- Search for, analysis and synthesis of data and information, with the use of the necessary technology
- Working independently
- Team Work
- Working in an international environment
- Production of new research ideas.
- Project planning and management
- Production of free, creative and inductive thinking

(3) SYLLABUS

Lectures:

1st: Introduction
Design Flow
EDA Tools 4
Translation of VHDL Code into a Circuit

2nd: Code Structure,
Fundamental VHDL Units
LIBRARY Declarations
ENTITY
ARCHITECTURE
Introductory Examples

3rd: Signals and Variables
Constants
Signals
Variables
Signal vs Variable

4th: Data Types and Operators
Pre-Defined Data Types
User-Defined Data Types

Arrays
Data Conversion
Operators
Properties
Examples

5th: Concurrent Code
Concurrent versus Sequential
Using Operators
WHEN (Simple and Selected)
GENERATE
Examples

6th: Sequential Code
PROCESS
IF
WAIT
CASE
LOOP
CASE versus IF
CASE versus WHEN
Clocking
Using Sequential Code to Design Combinational Circuits

7th: Circuit Designs' Examples
Sequential circuits' examples
Combinatorial circuits' examples

8th: Components and Packages
COMPONENT
PORT MAP
GENERIC MAP
Packages

9th: Finite State Machines (FSMs)
Design Style #1
Design Style #2 (Stored Output)
Alternatives design code for FSMs

10th: VHDL code for memories
VHDL code for RAMs
VHDL code for ROMs

11th: Code for synthesis and simulation
Test vectors
Code for testbenches
Combined VHDL codes' types
Code for synthesis

12th: Functions and Procedures
Function
Function Location
Procedure
Procedure Location
Function vs Procedure

13th: Additional System Designs
VHDL code examples for signal processing circuits, arithmetic circuits, shifters, data converters, etc.

Laboratories
The laboratory part of the course includes practical exercises that aim at the application and consolidation of the knowledge of the theory and concern:

1st: Adders (1-bit adder, addition with operator)

2nd: Parallel adder with structural description code

3rd: Counters

4th: Finite State Machines

5th: RAM and ROM memories

6th: Circuit and VHDL code of a simple arithmetic and logical unit

Attendance of laboratory exercises is mandatory.

(4) TEACHING and LEARNING METHODS - EVALUATION

<table>
<tr><td>DELIVERY
Face-to-face, Distance learning, etc.</td><td>Face to face in class and in the laboratory.
Distance learning support via e-Class system</td></tr>
<tr><td>USE OF INFORMATION AND COMMUNICATIONS TECHNOLOGY
Use of ICT in teaching, laboratory education, communication with students</td><td>• Slides (ppt) for teaching the theoretical part, which have been posted since the beginning of the semester in the e-Class.
• Laboratory guides for the laboratory part (one for each laboratory exercise), which have been posted on the e-Class since the beginning of the semester.
• Support of learning process through the e-Class platform (for notification of the course operating regulations, for distribution of slides, supplementary material, announcements, links and bibliography, for the conduct of the intermediate and final examination of the laboratory part, etc.).
• Specialized software e.g VIVADO for the laboratory part freely available to each student.</td></tr>
<tr><td>TEACHING METHODS

The manner and methods of teaching are described in detail.

Lectures, seminars, laboratory practice, fieldwork, study and analysis of bibliography, tutorials, placements, clinical practice, art workshop, interactive teaching, educational visits, project, essay writing, artistic creativity, etc.

The student's study hours for each learning activity are given as well as the hours of non-directed study according to the principles of the ECTS</td><td>
<table>
<tr><th>Activity</th><th>Semester workload</th></tr>
<tr><td>Lectures</td><td>26 (=13×2)</td></tr>
<tr><td>Seminars</td><td>13 (=13×1)</td></tr>
<tr><td>Laboratory Exercises (in Lab)</td><td>12 (=6x2)</td></tr>
<tr><td>Preparing Laboratory Exercises</td><td>26 hours</td></tr>
<tr><td>Lecture & bibliography study (at home)</td><td>48 hours</td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td>Course Total</td><td>125 hours (5 ECTS)</td></tr>
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<tr><td>STUDENT PERFORMANCE EVALUATION</td><td>A. Assessment of Theoretical Part:</td></tr>
</table>

Description of the evaluation procedure *Language of evaluation, methods of evaluation, summative or conclusive, multiple choice questionnaires, short-answer questions, open-ended questions, problem solving, written work, essay/report, oral examination, public presentation, laboratory work, clinical examination of patient, art interpretation, other* *Specifically-defined evaluation criteria are given, and if and where they are accessible to students.*	• Intermediate exam (30%), which includes solving exercises and multiple-choice questions with graded difficulty. • Written final exam (70%), that includes solving exercises, multiple choice questions and comparative evaluation of theory elements, graded difficulty. B. Evaluation of Laboratory Part: • Oral examination during laboratory exercises (40%) • Written final exam (60%) which includes solving exercises. <u>Remarks</u>: • The final grade results from the weighting of the theory and laboratory grades with weights of 60% and 40%, respectively. • The evaluation is done in the Greek language • The evaluation process and evaluation criteria are published on the course's website in the e-Class.

(5) ATTACHED BIBLIOGRAPHY

- *Suggested bibliography:*

In Greek
1) Volnei A. Pedroni, "Circuit Design with VHDL", Kleidarithmos, 2008.

2) Peter J Ashenden, "Digital Design: An Embedded Systems Approach Using VHDL", New Technologies Publisher, 2010.

3) Volnei A. Pedroni, “Circuit Design and Simulation with VHDL”, 2nd Edition, MIT Press, 2010.

4) David Harris and Sarah Harris, “Digital Design and Computer Architecture”, 2nd Edition, Morgan Kaufmann, 2012.